Comparing modelling methods

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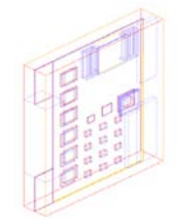
Comparing modelling methods

- The target assembly is on a 12-layer PCB
- FR-4 laminate with a conductor by volume ratio of 22%
- 12.4" high, 9" wide and 0.093" thick
- Maximum ambient temperature 50°C
- Maximum allowable component junction temperature 110°C
- Cooled by natural convection only



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This case study was one worked on by students on a Bolton University MSc module, but represents a very real product, a 12-layer PCB with a variety of components on it, many with thermal problems. This is a board for a telecommunications rack, and we will see the final rack in a later case study. At this stage, the simulation restricts itself to the board assembly, which uses a 12-layer board, with a significant amount of copper within it, and the requirement is for a maximum allowable junction temperature of 110°C in a maximum ambient of 50°C with cooling only by natural convection.

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The components

- 12-off 144-pin Plastic Quad Flat Packages (PQFP) dissipating 1.5W each (six on each side of the board)
- 12-off 28-pin Quad Plastic J-lead carrier chips (PLCC) dissipating 0.93W each
- 1-off 128-pin Plastic Thin Quad Flat Pack (TQFP) dissipating 1W
- 1-off 144-pin Plastic Quad Flat Pack dissipating 1.25W
- 1-off 35mm Plastic Ball Grid Array (BGA) dissipating 4W
- 1-off power supply brick with an extruded fin heat sink dissipating 13W
- Dissipation from other components 4W (assumed to be uniformly distributed on the PCB)

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The component list only identifies those components with a significant dissipation, and there are some 28 of these, with only a small contribution from other components.

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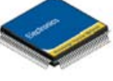
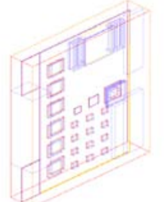


The components

- Overall dissipation ~52W
- Only a nominal layout at this stage
- Limited freedom of relocation
  - path length constraints



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Overall, the dissipation is around 52W, which is quite high for this size of board. But, as you will deduce from the form of the sketch, at this stage the components had only been placed in a nominal location, and the designer had some freedom to move them around on the board, within the usual high-frequency constraints of component proximity and restricted path lengths.

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<tr><td>

The components

- 12-off 144-pin Plastic Quad Flat Packages (PQFP) dissipating 1.5W each (six on each side of the board)
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The components include a number of different types of package, as well as a module. Not only does this give the students practice, but it represents reality!

The first task was to pull in typical values of thermal resistance for components in these packages, to create 2-resistor and DELPHI models, and then examine these with appropriate software. Of course, in a totally realistic application we would also be specifying which particular components are involved, because there will be slight differences in the construction, depending on the particular manufacturer.

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Comparing modelling methods

Initial evaluation
using representative package data

designator	package type	average ?$_{JA}$ (k/W)	P_D (W)	T_J (°C)
Q1–12	144-pin PQFP	37.9	1.5	106.9
Q13	128-pin PQFP	42.0	1	92.0
Q14	144-pin PQFP	37.9	1.25	97.4
Q15	35mm x 35mm BGA	24.7	4	148.8
Q16–27	28-pin PLCC	57.4	0.93	103.4

Calculated T_J figures based on average θ_{JA} figures

Note that $T_J = T_{amb} + (P_D \times \theta_{JA})$
where T_{amb} is the ambient temperature, 50°C

Based on this simple analysis, it can be seen that Q15 exceeds the maximum T_J figure of 110°C, whilst Q1?12 are running very close to this limit

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This is the initial evaluation carried out by one of our students using data for typical packages. This was a hand calculation, simplified by using a spreadsheet for the number crunching. Values of thermal resistance have been averaged from a number of sources, and used to predict the junction temperatures.

Whilst there are considerable variations in quoted thermal resistance for any package type, even an exercise as simple as this is useful in identifying those devices that require closer attention. You will see that Q1–12 are marginally below the maximum junction temperature, but Q15 is running well above specification.

Grateful thanks to Chris Hill of NXP for allowing us to quote significant elements from his work on this case study and the next one, *Modelling a small system*. Chris has also contributed to other parts of this project: there is an interview with him in *The need for thermal management* and he presents the tool demonstration in *How the tools work*.

Some issues

- Results highly dependent on test conditions – the actual environment will be different from that in which the θ_{JA} measurements were made.
- Quoted θ_{JA} figures do not allow for multiple heat-dissipating devices mounted in close proximity
  - there will inevitably be thermal "cross-coupling"
  - all devices will experience higher temperature rises than if they were operating in isolation

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Of course, using representative package data is dangerous, because θ_{JA} results in particular are highly dependent on the test conditions. Even if JEDEC tests have been used, the local environment is likely to be different from the standard environment used for the θ_{JA} measurements.

In particular, the θ_{JA} parameters quoted will be for isolated components, not for many heat-dissipating parts mounted close together. And we would expect that there will be thermal "cross-coupling", so that all the devices will experience higher temperature rises than if they were operating in isolation.

Some issues

- Results highly dependent on test conditions – the actual environment will be different from that in which the θ_{JA} measurements were made.
- Quoted θ_{JA} figures do not allow for multiple heat-dissipating devices mounted in close proximity
- Quoted θ_{JA} figures do not
  - allow for the application of heat-sinks, fans and other cooling aids
  - take account of the likelihood that the board will be mounted in some form of enclosure
    - this will have an impact on the airflow around the devices, and hence on their operating temperatures

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The θ_{JA} figures will be for an isolated device naturally cooled, so they do not take into account heat sinks, fans or other cooling aids. They also assume free air movement, whereas, in the end-user application, the board will almost certainly be mounted in some form of enclosure that will have an impact on the airflow around the devices, and hence on their operating temperatures.

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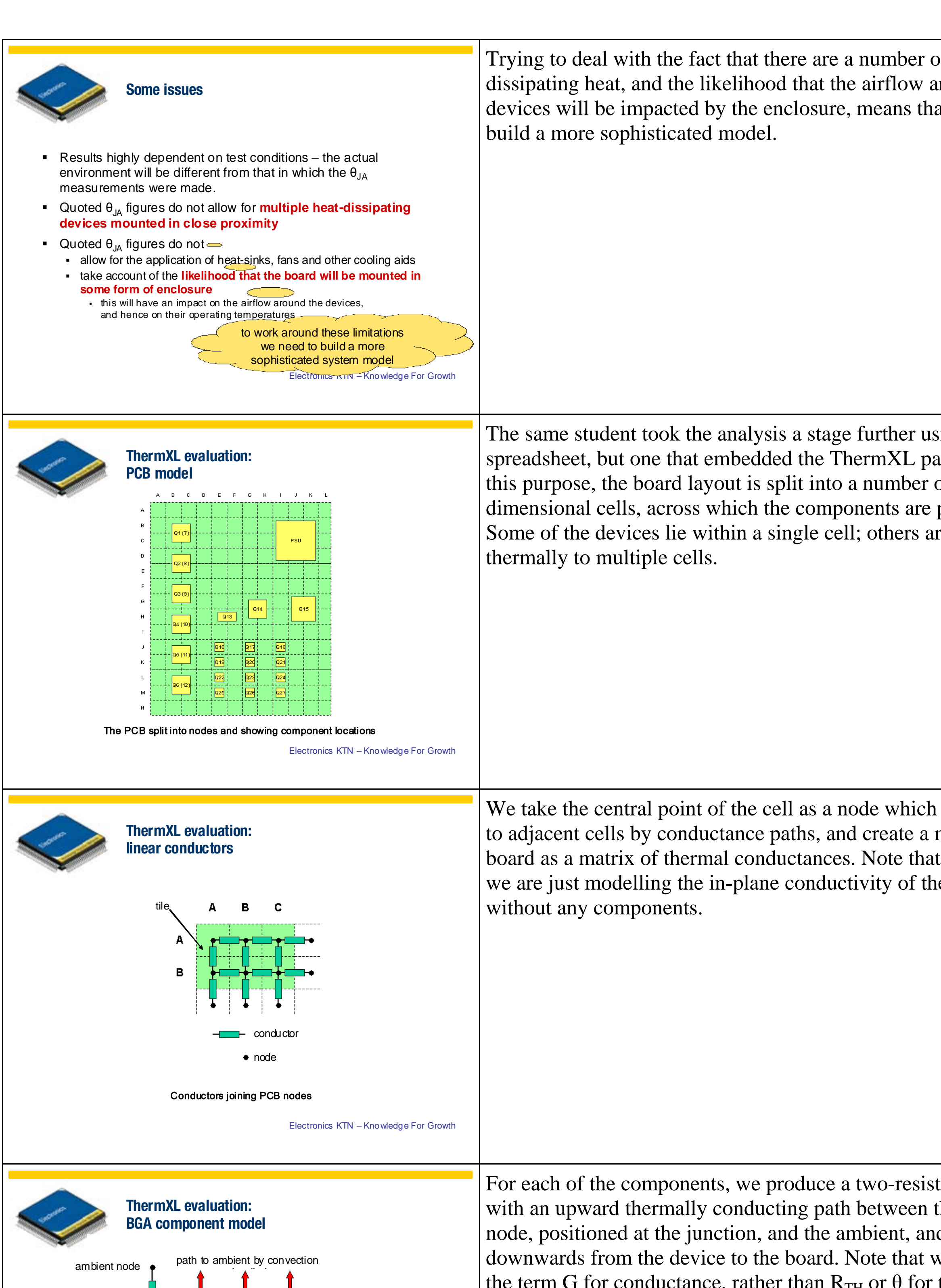

Trying to deal with the fact that there are a number of devices dissipating heat, and the likelihood that the airflow around these devices will be impacted by the enclosure, means that we need to build a more sophisticated model.

The same student took the analysis a stage further using a spreadsheet, but one that embedded the ThermXL package. For this purpose, the board layout is split into a number of two-dimensional cells, across which the components are positioned. Some of the devices lie within a single cell; others are related thermally to multiple cells.

We take the central point of the cell as a node which is connected to adjacent cells by conductance paths, and create a model of the board as a matrix of thermal conductances. Note that at this stage we are just modelling the in-plane conductivity of the board without any components.

For each of the components, we produce a two-resistor model, with an upward thermally conducting path between the device node, positioned at the junction, and the ambient, and then downwards from the device to the board. Note that we are using the term G for conductance, rather than R_{TH} or θ for thermal resistance.

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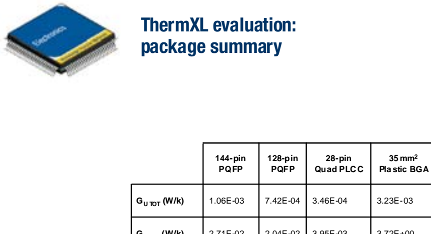
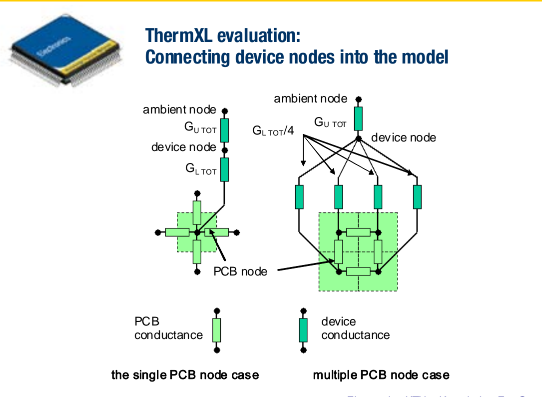


	144-pin PQFP	128-pin PQFP	28-pin Quad PLCC	35 mm² Plastic BGA
$G_{U\,TOT}$ (W/k)	1.06E-03	7.42E-04	3.46E-04	3.23E-03
$G_{L\,TOT}$ (W/k)	2.71E-02	2.04E-02	3.95E-03	3.72E+00

$G_{U\,TOT}$ and $G_{L\,TOT}$ summary by package type

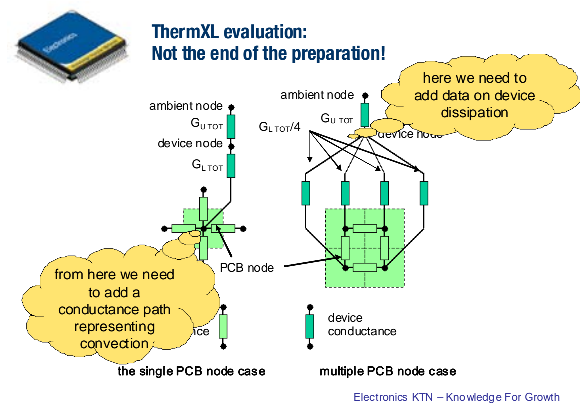
This table shows the calculated values for thermal conductance for each of the different types of package. Note that a very small thermal conductance is the same as a large value of thermal resistance. These values were calculated from scratch using the bulk materials and their dimensions, but most ThermXL evaluations will of course use published figures.

ThermXL evaluation:
Connecting device nodes into the model

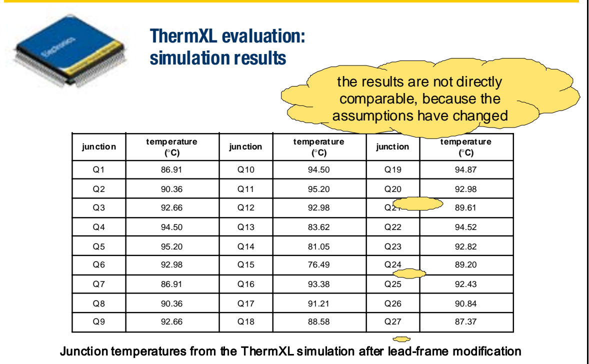


Where the device is connected just to a single cell on the board, we use the type of connection shown in the left-hand part of the diagram. Where a device disperses heat into more than one node, we use the approach indicated in the right-hand part of the diagram, where the conductance of the whole package is divided by the number of cells. So, in the case of the PSU, which extends over nine cells, the value of conductance associated with each cell would be one-ninth of the total junction to board conductance. This isn't the only way of tackling the problem, but it ties in fairly closely with reality.

ThermXL evaluation:
Not the end of the preparation!



This isn't the end of the preparatory work, because we still need to add data on the device dissipation at the device node, and conductance paths from each board node representing the heat loss by convection. While this seems tedious, it has the great advantage that it forces the thermal designer to understand in detail what is happening.



junction	temperature (°C)	junction	temperature (°C)	junction	temperature (°C)
Q1	86.91	Q10	94.50	Q19	94.87
Q2	90.36	Q11	95.20	Q20	92.98
Q3	92.66	Q12	92.98	Q21	89.61
Q4	94.50	Q13	83.62	Q22	94.52
Q5	95.20	Q14	81.05	Q23	92.82
Q6	92.98	Q15	76.49	Q24	89.20
Q7	86.91	Q16	93.38	Q25	92.43
Q8	90.36	Q17	91.21	Q26	90.84
Q9	92.66	Q18	88.58	Q27	87.37

Junction temperatures from the ThermXL simulation after lead-frame modification

The final stage is to use the ThermXL add-in to generate the results, which requires some iteration, but quickly yields a set of predictions of the thermal situation that can be tabulated as above, or converted into graphical form. The results are distinctly different from the first pass, but the figures here have been distorted by assumptions made about the internal structure. The purpose of showing the work is to indicate the method, not comment on the results.

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Comparing modelling methods

Slide	Commentary

Device models using FLOPACK – 1
▪ FLOPACK is a web-based product from Flomerics designed to generate accurate thermal models of IC components, test boards, standard test harnesses and other associated parts with the minimum of input
▪ Inbuilt model creation utility can generate
  ▪ detailed models
  ▪ 2R models
  ▪ DELPHI models
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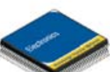
	Having gained an understanding of the thermal paths, and estimated the results, our student then modelled the components within FLOPACK. This is a web-based product, designed to generate thermal models of circuit elements with the minimum of input.
	The utility creates a detailed model, from which it can generate different types of compact model, including two-resistor and DELPHI models.

Device models using FLOPACK – 2 ▪ FLOPACK can also access a collection of “Smart Part” modules installed on a central web server ▪ Smart Parts encapsulate in-built common industry manufacturing and design rules used by most IC component suppliers ▪ These rules will generate a reasonably accurate package model from a reduced set of input parameters Electronics KTN – Knowledge For Growth	In many cases the tool will contain manufacturer’s information about the part, but FLOPACK can also access a collection of “SMART part modules”. These are macros that allow you to create a model quite simply, by inputting information about the component of interest. The macros are based on the design rules and materials used by most IC suppliers, so will generate a reasonably accurate package model, even though there may be gaps in the data set.
 **PCB simulation using FLO/PCB** ▪ FLO/PCB is a simulation program for concept development of printed circuit assemblies ▪ Derives physical layout directly from the functional block diagram ▪ Fully-integrated library capability supports JEDEC standards for component thermal models Electronics KTN – Knowledge For Growth	But FLOPACK only creates a model of the component. We could use this in hand calculations, or in ThermXL, but here we have chosen instead to use the package information and feed it into FLO/PCB, a simulation programme that is designed for the concept development of printed circuit assemblies. The starting point is information about the board, but the physical layout can be derived directly from the functional block diagram. The thermal model of each component is available from a component library that supports JEDEC standards, or the information can be fed in from the SMART parts created by FLOPACK.
PCB simulation using FLO/PCB ▪ FLO/PCB is a simulation program for concept development of printed circuit assemblies ▪ Derives physical layout directly from the functional block diagram ▪ Fully-integrated library capability supports JEDEC standards for component thermal models ▪ CFD-based 3D solver predicts airflow and temperature for both sides of the board Electronics KTN – Knowledge For Growth	The product works in three dimensions, and uses the same iterative solution approach as more sophisticated packages to predict the airflow and temperature on both sides of the board. Simplified “cut down” packages of this type are well suited to the “what if” requirements of a designer, because the model development is shorter, and solutions available much more quickly.

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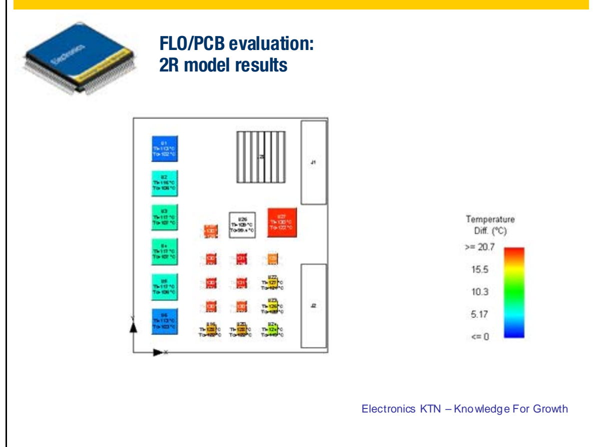
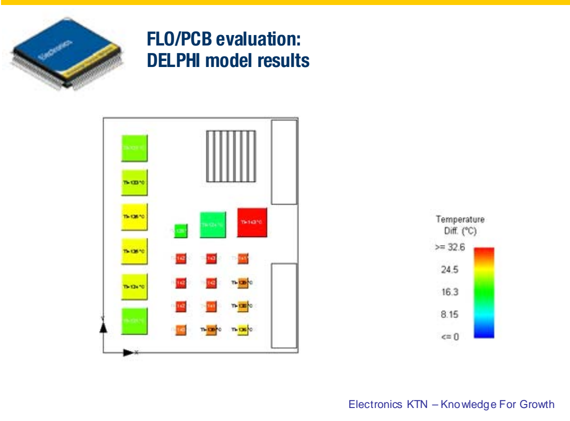
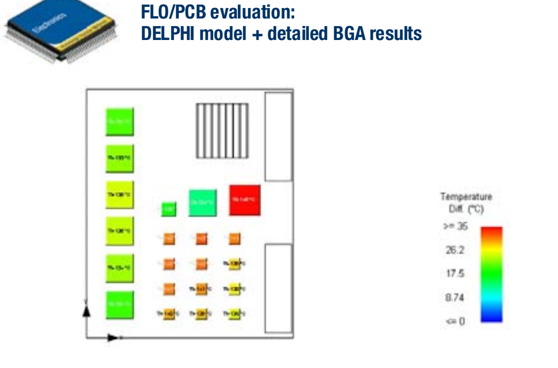
Comparing modelling methods



The normal style of presentation is graphical, and here we can see the distribution of heat over the board. For each package we have junction temperature and case temperature, and this is shown by component colour. But notice that in this case even the blue ones are quite hot! The legends are difficult to read, but Q15 is shown as having a temperature of 130°C, based on the two-resistor model.



When we substitute DELPHI model results, we see a much larger temperature range, with a BGA package (Q15) predicted as reaching 143°C. It is interesting to note how close this came to the original hand calculation, which was based on a simple equation, with the temperature rise at the junction being the ambient temperature plus the product of the thermal resistance and the power dissipation.



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Importing the detailed model for the critical component, we find that the predicted temperature has increased by a further 2°C, to 145°C as against 143°C. So the DELPHI model is, as predicted, giving a very similar result to the detailed model, but the two-resistor model is significantly different.

- Separate the PQFPs so that the six on the bottom side and the six on the top side are not directly opposite each other
- Stagger the PLCCs to give more space between them
- Move the PBGA towards the centre of the two connectors where the board temperature is at its lowest

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All our models have shown that some of the parts are getting too hot, and one particularly so. So the challenge is to make changes to the design in order to improve it thermally. The remit was to use only natural convection, so only a rearrangement of components was possible.

The decisions suggested, which of course in real life would need validation from the electronic design point of view, were:

- to separate heat generating components so that top side and bottom side parts were not directly opposite each other
- stagger the other components to give more space, and
- move the critical PBGA to an area where the board temperature is at its lowest.

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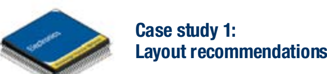
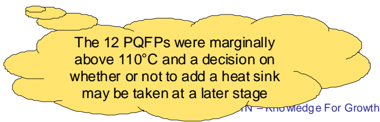
Comparing modelling methods



Case study 1:
Layout recommendations

- Separate the PQFPs so that the six on the bottom side and the six on the top side are not directly opposite each other
- Stagger the PLCCs to give more space between them
- Move the PBGA towards the centre of the two connectors where the board temperature is at its lowest
- Move the power supply to the top of the board
- Add heat sinks to the PBGA, PLCCs and the TQFP



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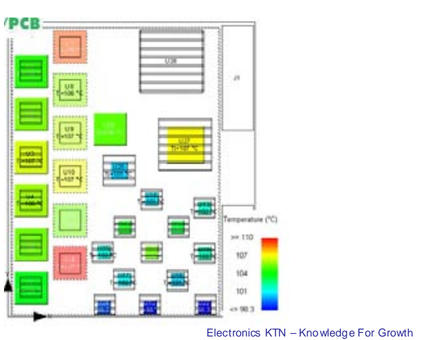
We allowed the power supply to be relocated, so this was moved to the top. [Of course, in a multi-board situation, one might look for alternatives]

In this case it was also possible to add heat sinks to key components, and re-run the simulation once again.

The junction temperatures of some components are close to the maximum operating temperature, which is not surprising with a board with this total dissipation, and only natural cooling. And the simulation showed that some components were actually marginally over the allowable temperature. The need to deal with these issues has to be identified early as it will need consideration at a later stage.

Case study 1:
FLO/PCB evaluation: final layout



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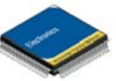
The final layout shows that the requirements have been broadly met, although significant numbers of heat sinks were necessary. In practice of course products of this sort would be given forced convection cooling.



Conclusions on the methods

- All the changes could be modelled
  - the simulation tool rapidly produced something with reasonable accuracy
  - using DELPHI models cut the time significantly
- Benefits
  - allowing the design to be developed, and changes evaluated in several stages
  - "what if" analysis makes simulation particularly powerful
- Bear in mind the limitations of the technique
  - explore the use of different tools
  - carry out "sanity checks" by calculation from first principles
  - it remains only a *simulation*, and needs to be validated

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The point of course is that using a simulation tool rapidly produced something that appeared to mimic the real world to reasonable accuracy. Using DELPHI models cut the time significantly, allowing the design to be developed, and changes evaluated in several stages. So intuition could be supported by modelling, and it is this "what if" analysis that makes simulation particularly powerful.

But at all times one has to bear in mind the limitations of the technique, and it is always worth exploring the use of different tools, and in particular carrying out "sanity checks" by calculation from first principles, if only to give the user confidence that the results obtained are likely to be reliable. But it remains only a simulation, and eventually the product will need to be made, its performance measured, and the simulation validated.

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