











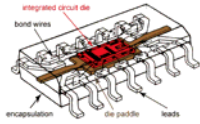



# Modelling heat-generating elements

 <h3>Modelling heat-generating elements</h3> <ul style="list-style-type: none"><li>▪ Modelling heat flow paths</li><li>▪ Component packaging – an overview</li><li>▪ Applying thermal resistance concepts to the package</li><li>▪ Thermal parameter measurement</li><li>▪ Thermal models<ul style="list-style-type: none"><li>▪ 2R model</li><li>▪ compact models</li><li>▪ DELPHI models</li><li>▪ detailed models</li></ul></li><li>▪ How these models compare</li></ul> <p>Electronics KTN – Knowledge For Growth</p>	<p>Having reviewed in the previous section some of the modelling basics, and introduced the idea of thermal resistance, in this section of the presentation we look in more detail at the way in which heat-generating elements are modelled. As part of this we will be examining package structures and how thermal resistance concepts apply to the package before moving on to thermal parameter measurement and the development of different types of thermal model.</p>
 <h3>Modelling heat flow paths – 1</h3> <ul style="list-style-type: none"><li>▪ Components generate significant heat!</li><li>▪ From a design perspective it is important to:<ul style="list-style-type: none"><li>▪ get the heat out quickly</li><li>▪ get the cold in quickly</li><li>▪ avoid costly over-design</li></ul></li></ul> <p>Electronics KTN – Knowledge For Growth</p>	<p>Whilst in a high current situation the actual interconnections might get hot, most of the heat in an electronic circuit is generated by the components, and in most cases the <math>I^2R</math> (or “Joule”) heating is concentrated within the semiconductors, in particular complex integrated circuits such as microprocessors and graphics chips, and power semiconductors.</p> <p>From the design point of view it is important to dissipate that heat, using heat sinks, fans and other strategies to move heat from its source into the environment – we want to get the cold in quickly! At the same time it is important to do only what is necessary, as cooling can cost money, and often it is possible to avoid expense just by rearranging or repositioning things to make thermal improvements.</p>
 <h3>Modelling heat flow paths – 1</h3> <ul style="list-style-type: none"><li>▪ Components generate significant heat!</li><li>▪ From a design perspective it is important to:<ul style="list-style-type: none"><li>▪ get the heat out quickly</li><li>▪ get the cold in quickly</li><li>▪ avoid costly over-design</li></ul></li><li>▪ From a simulation perspective it is important to:<ul style="list-style-type: none"><li>▪ model the critical heat flow paths accurately</li><li>▪ so that the designer can<ul style="list-style-type: none"><li>▪ deal adequately with any thermal challenges</li><li>▪ examine the thermal effects of changes</li></ul></li></ul></li></ul> <p>Electronics KTN – Knowledge For Growth</p>	<p>From the simulation perspective, what we are trying to do is model the critical heat flow paths accurately, concentrating on the main sources of heat. The model needs to be accurate enough to allow the designer both to deal adequately with any thermal challenges and to examine the effects of design changes.</p> <p>Simulations are very useful for carrying out “what if” analysis at the product development stage and helping the designer to answer the questions that simplistically might be expressed as: Should I put a fan in the box? Or more than one fan? Should I change or move the power supply? Or even: Should I knock another hole in the side of the box?!</p>
 <h3>Modelling heat flow paths – 2</h3> <ul style="list-style-type: none"><li>▪ This relies on being able to create a model of the thermal paths that gives us precise information on the resistance to thermal flow as heat leaves by<ul style="list-style-type: none"><li>▪ conduction (removal through a solid body)</li><li>▪ convection (removal by air)</li><li>▪ radiation (through EM transfer from solid &gt; solid)</li></ul></li></ul> <p>Electronics KTN – Knowledge For Growth</p>	<p>In order to answer the question of how heat should be most effectively removed, we need to be able to create a model of the thermal paths that gives us precise information on the resistance to thermal flow as heat leaves the junction by conduction through the body of the device through to the surface and the leads, conduction away from the device through the board, and convected heat from the device surface and board into the ambient.</p> <p>We need to look at all the mechanisms for device and substrate, taking into account any heat sinks or fans used within the system. Typically the thermal modelling and simulation will focus on conduction and convection, because loss of heat by radiation is often small enough to disregard.</p>

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 <h3>Modelling heat flow paths – 2</h3> <ul style="list-style-type: none"><li>▪ This relies on being able to create a model of the thermal paths that gives us precise information on the resistance to thermal flow as heat leaves by<ul style="list-style-type: none"><li>▪ conduction (removal through a solid body)</li><li>▪ convection (removal by air)</li><li>▪ radiation (through EM transfer from solid &gt; solid)</li></ul></li><li>▪ The thermal designer needs to know for each device<ul style="list-style-type: none"><li>▪ the heat dissipated</li><li>▪ its thermal characteristics</li><li>▪ often these are expressed in terms of thermal resistances</li></ul></li></ul> <p>Electronics KTN – Knowledge For Growth</p>	<p>The thermal designer needs to know, at least for the most significant devices within an assembly, the heat that is dissipated, and the thermal characteristics of the package. Often these will be expressed in terms of thermal resistance.</p>
 <h3>A Caveat</h3> <ul style="list-style-type: none"><li>▪ Importance of good input data</li></ul> <p>Electronics KTN – Knowledge For Growth</p>	<p>It is worth saying at this stage the input data should be as good as we can possibly get it, and this needs to reflect the application, rather than rely on maximum limits within the published data. A device may be rated at 300mW, yet dissipate only a few percent of that within the circuit. If you add worse case for everything, then the thermal design could end up far too conservative.</p>
 <h3>A Caveat</h3> <ul style="list-style-type: none"><li>▪ Importance of good input data</li><li>▪ Limitations of published data<ul style="list-style-type: none"><li>▪ power dissipation</li><li>▪ thermal resistances</li></ul></li><li>▪ Thermal resistance data<ul style="list-style-type: none"><li>▪ how reliable?</li><li>▪ how accurate?</li><li>▪ how derived?</li><li>▪ the effect of boundary conditions</li></ul></li></ul> <p>Electronics KTN – Knowledge For Growth</p>	<p>Power dissipation is a figure that will be quoted by the package manufacturer, and can be estimated by the designer, or even measured. Thermal resistances are more difficult to obtain, though manufacturers will often quote them. As we will see, the figures might derive from an inadequate thermal model, or be measured under standard conditions that don't reflect reality. In particular, we have to be aware that changing the boundary conditions can affect the thermal data – even putting a heat sink on a component will significantly affect its characteristics. But to some extent we are jumping ahead, so let's return to the basics of our model.</p>
 <h3>The source of the heat</h3> <ul style="list-style-type: none"><li>▪ The part that consumes electrical power (= generates heat) in a semiconductor device is the junction</li><li>▪ The heat that is generated at the junction propagates through the internal structure of the device and reaches its surface (case) and leads<ul style="list-style-type: none"><li>▪ the same arguments also apply to passive devices</li></ul></li></ul> <p>Electronics KTN – Knowledge For Growth</p>	<p>We've focused on semiconductors because they are active components, they are drawing current from the power supply, they are processing data, and in most cases the semiconductors are the major generators of heat within the system. But that heat is being generated within the device at the junctions, which are buried within the structure.</p> <p>In the case of a semiconductor, the heat from the junction propagates from the die, through the die paddle and eventually through to the leads and the outside of the case. And something similar also applies to passive devices, where the heat-generating elements are internal, although they may be differently distributed from the semiconductor.</p>


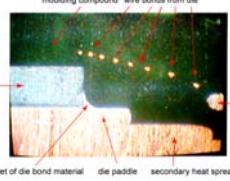

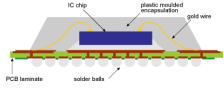



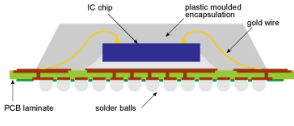

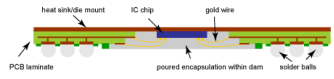

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 <p><b>Component packaging: Lead-frame device</b></p> <ul style="list-style-type: none"> <li>▪ Die is attached to a 'paddle' or 'flag' on a lead frame</li> <li>▪ Provides a thermal (and usually electrical) path to the die reverse</li> <li>▪ Connections are made between the die surface and the lead-frame by wire bonding</li> </ul>  <p style="text-align: center;"><small>Electronics KTN – Knowledge For Growth</small></p>	<p>We'll look first at a conventional integrated circuit, in this case a simple 14-lead package containing a small-scale integrated device. The die is sitting on the central section of the lead-frame referred to as the "paddle", to which it is attached, usually by conductive adhesive. Connections to the lead-frame are made with gold or aluminium wires, and the overall package ...</p>
 <p><b>Component packaging: Lead-frame device</b></p> <ul style="list-style-type: none"> <li>▪ Die is attached to a 'paddle' or 'flag' on a lead frame</li> <li>▪ Provides a thermal (and usually electrical) path to the die reverse</li> <li>▪ Connections are made between the die surface and the lead-frame by wire bonding</li> <li>▪ Package completed by transfer-moulding of an encapsulation material, usually a modified epoxy</li> <li>▪ The lead-frame is plated, cropped and formed, ready for coding and final testing</li> </ul>  <p style="text-align: center;"><small>Electronics KTN – Knowledge For Growth</small></p>	<p>... is completed by transfer moulding an encapsulation material, which is usually a modified epoxy. The final stage in the process is to plate the lead frame, and crop and form, ready for coding and final testing, but these stages, while visible and important, do not affect the thermal performance of the package.</p>
 <p><b>Component packaging: Lead-frame device</b></p> <ul style="list-style-type: none"> <li>▪ Factors internal to the package that affect the thermal resistance from package to ambient include:             <ul style="list-style-type: none"> <li>▪ layout density of chip</li> <li>▪ the <i>material</i> used by the lead-frame                 <ul style="list-style-type: none"> <li>▪ trend to copper replacing Alloy 42</li> </ul> </li> <li>▪ the <i>design</i> of the lead-frame                 <ul style="list-style-type: none"> <li>▪ tie bar size and die pad size are most significant factors</li> <li>▪ size and shape of leads has lesser effect</li> </ul> </li> </ul> </li> </ul> <p style="text-align: center;"><small>Electronics KTN – Knowledge For Growth</small></p>	<p>Factors internal to the package that affect the thermal resistance and package ambient include the layout density of the chip, but most important are the material and design of the lead-frame. The traditional material was Alloy 42, but there has been a trend to use copper to replace it. This is fortunate from the thermal point of view, because copper has about five times the conductivity of Alloy 42!</p> <p>The design of the lead-frame is also important, and circuits can vary widely in how much metal is present, the most important features in a design being the tie bar and die pad, that is the elements of the lead-frame that are closest to the die, and can help move heat away from the junction. The size and shape of the lead has a lesser effect.</p>




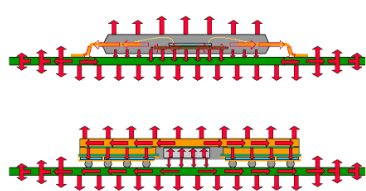
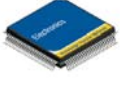
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 <p><b>Component packaging: Lead-frame device</b></p> <ul style="list-style-type: none"> <li>Factors internal to the package that affect the thermal resistance from package to ambient include: <ul style="list-style-type: none"> <li>layout density of chip</li> <li>the <i>material</i> used by the lead-frame <ul style="list-style-type: none"> <li>trend to copper replacing Alloy 42</li> </ul> </li> <li>the <i>design</i> of the lead-frame <ul style="list-style-type: none"> <li>tie bar size and die pad size are most significant factors</li> <li>size and shape of leads has lesser effect</li> </ul> </li> <li>the moulding compound</li> <li>whether a heat spreader is used within the package</li> </ul> </li> </ul> <p style="text-align: right;">Electronics KTN – Knowledge For Growth</p>	<p>Although there is an enormous difference in conductivity between the copper of the lead-frame and the encapsulation material, the moulding compound still has some part to play.</p> <p>Unfortunately there is limited scope for major enhancement, as loading the compound to improve the thermal conductivity of the basic resin tends to reduce adhesion. There also is a limit to how much filler can be added because the transfer moulding process needs the material to be fairly fluid when hot.</p> <p>We can, however, add extra copper within the package as a “heat spreader”, and this can have a very significant impact on thermal performance.</p>
 <p><b>Component packaging: Lead-frame device</b></p> <ul style="list-style-type: none"> <li>Factors <i>external</i> to the package, but which are related to the package design and application, include: <ul style="list-style-type: none"> <li>package–substrate gap</li> <li>availability of a flat surface for heat-sinking</li> <li>heat transfer compounds</li> <li>copper tracks on board</li> <li>external cooling devices designed to be attached to the package (such as fans and Peltier devices)</li> </ul> </li> </ul> <p style="text-align: right;">Electronics KTN – Knowledge For Growth</p>	<p>The thermal performance of a component is also influenced by design decisions made about both the outer package and the application where it is being used. To give a short list of some of those – we can choose the design gap between package and substrate, the design of the pads and tracks on the board and any vias associated with the pads, whether a flat surface is available for ease of heat sinking, and whether thermal interface materials will be used for heat transfer between package and conductive surfaces on board or heat sink. And for some parts, the package provider will also specify (and sell you) external local cooling devices designed to be attached to the package, such as fans and thermoelectric cells.</p>
 <p><b>Not always what they seem</b></p> <ul style="list-style-type: none"> <li>Substantial variations in package design</li> <li>A typical example:  </li> </ul> <p style="text-align: right;">Electronics KTN – Knowledge For Growth</p>	<p>Bear in mind that things aren’t always as they seem. You can’t control what is in the package, and a worse problem is that you don’t really know what is in the package and there may be variations between suppliers, where what is apparently the same product will function the same electrically, but be different thermally.</p> <p>The picture shows an example of a product that was sectioned – you can see the silicon die, a small fillet of conductive epoxy used as a die bond material, and the die paddle. The die paddle is in a plane just below the leads, where you would expect it to be, and there are signs of the wire bonds between die and leads. They are relatively small, probably 28µm wire, so play little part in the thermal equation.</p>
 <p><b>Not always what they seem</b></p> <ul style="list-style-type: none"> <li>Substantial variations in package design</li> <li>A typical example:  <ul style="list-style-type: none"> <li>separate thermal plane of copper</li> <li>separated from the die by the die paddle</li> <li>presence totally unsuspected until device sectioned!</li> </ul> </li> </ul> <p style="text-align: right;">Electronics KTN – Knowledge For Growth</p>	<p>What does play a very significant part is the secondary heat spreader, a substantial lump of copper underneath the die paddle. This makes no difference to the electrical performance of the part, but its thermal mass, and its closeness to the external surface will make a considerable difference to the thermal performance. This is something that you could not possibly have predicted from the outside, and it would be fairly certain if you were buying the product from another vendor it would be different.</p>





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 <p><b>Not always what they seem</b></p> <ul style="list-style-type: none"> <li>Substantial variations in package design</li> <li>A typical example</li> </ul> <p>understanding the internals of the device helps us understand its limitations</p>  <ul style="list-style-type: none"> <li>separate thermal plane of copper</li> <li>separated from the die by the die paddle</li> <li>presence totally unsuspected until device sectioned!</li> </ul> <p><small>Electronics KTN – Knowledge For Growth</small></p>	<p>The main route for heat is still through the encapsulation material to the leads, but the thermal path is enhanced by the larger heat spreader, and inevitably the distance between the bottom of the heat spreader and the bottom of the package will be much reduced.</p> <p>What is slightly surprising about the package is that the spreader was not taken to the outside of the package, so there are still thermal limitations. Ideally the spreader should penetrate the surface of the package, so that it can be attached to the board or heat sink, preferably using an effective thermal interface material.</p> <p>Note how understanding the internals of the device helps us to understand its limitations.</p>
 <p><b>Area arrays</b></p>  <ul style="list-style-type: none"> <li>Lead-frame replaced by substrate</li> <li>Connections <ul style="list-style-type: none"> <li>from die by wire bonds</li> <li>through vias in the substrate</li> <li>to solder balls (or equivalent) on underside</li> </ul> </li> <li>Encapsulation <ul style="list-style-type: none"> <li>usually provided by transfer moulding</li> </ul> </li> </ul>   <p><small>Electronics KTN – Knowledge For Growth</small></p>	<p>For the high pin counts typical of microprocessors and similar devices, where a lead-frame is not practicable, integrated circuits are typically packaged in one of several styles of “area array” of which the one illustrated is the original OMPAC. The lead-frame has been replaced by an “interposer”, usually a printed circuit board made in a glass reinforced plastic, though there are ceramic variants. Connections are made using vias through the interposer, and the thermal and electrical path is through solder balls (or sometimes columns) on the underside.</p> <p>Encapsulation for this style of array is provided by transfer moulding, . . .</p>
 <p><b>Face-up construction</b></p> <ul style="list-style-type: none"> <li>Thermal path <ul style="list-style-type: none"> <li>most heat exits through the balls <ul style="list-style-type: none"> <li>extended path</li> <li>low-conductance substrate</li> <li>via conduction becomes very important</li> </ul> </li> <li>little through the top surface of the package</li> </ul> </li> <li>Need to modify the package to improve thermal performance</li> </ul>  <p><small>Electronics KTN – Knowledge For Growth</small></p>	<p>. . . but the plastics used have very much lower thermal conductivity than metals. As a result, whilst some heat goes to the surface, most leaves the package through the balls. The thermal path is extended, and the substrate is of low conductivity, so that via conduction becomes very important. If the package encloses a chip with high dissipation, it will run hot, and we need to modify the design in order to improve the thermal performance.</p>
 <p><b>Face-down construction</b></p> <ul style="list-style-type: none"> <li>Schematic internal construction and general view of a ‘tape BGA’</li> </ul>   <p><small>Electronics KTN – Knowledge For Growth</small></p>	<p>In this case, the internal structure has been inverted, so that the chip is mounted direct on the metal top surface of the package, with electrical connection made using a multilayer interposer from wire bond to interposer, and then from interposer through balls to the support substrate. This type of “Tape BGA package” has the great advantage that the IC chip can be very closely thermally bonded to an extended surface that acts as a heat spreader.</p>





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 <p><b>Face-down = die reverse up</b></p> <ul style="list-style-type: none"> <li>The main thermal path in the Tape BGA is to the top surface of the package</li> <li>Adding a simple heat sink is relatively easy</li> <li>This type of package is frequently employed for devices with high power dissipation</li> </ul> <p style="text-align: right; font-size: small;">Electronics KTN – Knowledge For Growth</p>	<p>The Tape BGA package has thus been designed with good thermal performance in mind, and the fact that the main thermal path is to the top surface means that adding a heat sink is relatively easy. In consequence, this type of package is frequently used for devices with high power dissipation such as processors or graphics chips.</p>
 <p><b>Face-down = die reverse up</b></p> <ul style="list-style-type: none"> <li>The main thermal path in the Tape BGA is to the top surface of the package</li> <li>Adding a simple heat sink is relatively easy</li> <li>This type of package is frequently employed for devices with high power dissipation</li> <li>Many different options, including ceramic packages</li> </ul> <p style="text-align: right; font-size: small;">Electronics KTN – Knowledge For Growth</p>	<p>I must emphasise that the packages described are generic styles and there are many different options available, including ceramic packages. In every case it is important to understand the construction, because the heat paths through the package depend on that construction. A vital thing to remember is that there are potentially many different package types for the same electrical function, and these will have different thermal characteristics. When you have a challenging thermal situation, you need to make sure that your selection is on both thermal and electronic grounds.</p>
 <p><b>Package heat flow patterns</b></p> <ul style="list-style-type: none"> <li>Heat flow patterns for face-up and face-down packages</li> </ul>  <ul style="list-style-type: none"> <li>Will involve conduction and convection</li> </ul> <p style="text-align: right; font-size: small;">Electronics KTN – Knowledge For Growth</p>	<p>The heat flows for face-up and face-down chips are different, and this has been illustrated here. Heat moves laterally through conductors, both in the package and in the board itself, but it is also lost from the surfaces by convection.</p>
 <p><b>Detailed thermal model – 1</b></p> <ul style="list-style-type: none"> <li>A detailed model             <ul style="list-style-type: none"> <li>attempts to represent or reconstruct the physical geometry of a package to the greatest feasible extent</li> <li>will physically appear similar to the actual package geometry</li> </ul> </li> <li>The detailed model             <ul style="list-style-type: none"> <li>breaks down the structure into small elements                 <ul style="list-style-type: none"> <li>material homogenous throughout the element</li> </ul> </li> </ul> </li> </ul> <p style="text-align: right; font-size: small;">Electronics KTN – Knowledge For Growth</p>	<p>In our last slide some of the heat flow paths were illustrated superimposed on a representation of the actual package. Our starting point for modelling will be what is referred to as a “detailed model” which tries to mimic as accurately as possible the real thing, in every sense.</p> <p>This model appears physically similar to the actual package geometry, and internally the structure will be broken down into small elements, each of which is made of homogenous material, so that its characteristics can be calculated.</p>





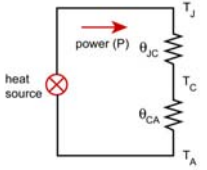
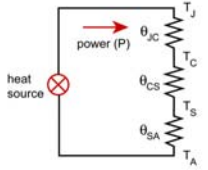
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 <p><b>Detailed thermal model – 2</b></p> <ul style="list-style-type: none"><li>▪ The results of the model can be used as our benchmark</li><li>▪ Detailed thermal models<ul style="list-style-type: none"><li>▪ suitable for the simulation of designs with few packages</li><li>▪ not feasible for system-level computations that involve a large number of semiconductor packages<ul style="list-style-type: none"><li>▪ require a significantly large computational effort!</li></ul></li></ul></li><li>▪ Resultant effort to produce simpler models</li></ul> <p>Electronics KTN – Knowledge For Growth</p>	<p>Because the information is in considerable detail, the results of the model can be used as our benchmark for comparisons. Detailed thermal models alone can be used in simulations with few packages, but aren't feasible for system-level computations that involve a large number of heat sources, because representing each package by a detailed model requires a significantly large computational effort.</p> <p>The result is that considerable efforts have been expended to produce models that are simpler, yet adequately accurate.</p>
 <p><b>Compact thermal model</b></p> <ul style="list-style-type: none"><li>▪ A compact thermal model aims at accurate prediction of package temperature only at selected key points: junction, case and leads<ul style="list-style-type: none"><li>▪ and without excessive computational effort</li></ul></li><li>▪ A compact model will generally use a thermal resistor network to represent the thermal paths and mimic the <i>behaviour</i> of the component rather than its geometry and material properties<ul style="list-style-type: none"><li>▪ it won't look like the part, but it will model the response of the part to its thermal environment</li></ul></li></ul> <p>Electronics KTN – Knowledge For Growth</p>	<p>What is sometimes referred to as a “compact thermal model” aims to avoid excessive computational effort by restricting its efforts to predicting accurately the package temperature at selected key points, normally junction, case and leads.</p> <p>A compact model will generally use a thermal resistor network, so it looks nothing like the part, but by representing the thermal paths the network allows the user to model the response of the part to its thermal environment. So the compact model mimics the behaviour of the component rather than its geometry and material properties.</p>
 <p><b>Simpler models</b></p> <ul style="list-style-type: none"><li>▪ In a semiconductor device<ul style="list-style-type: none"><li>▪ the source of heat is the junction</li><li>▪ the heat generated propagates through the internal structure of the device and reaches its surface and leads</li><li>▪ that heat is released into the environment by both conduction and convection</li></ul></li><li>▪ The simplest models have:<ul style="list-style-type: none"><li>▪ a single thermal resistance from junction to surroundings</li><li>▪ thermal resistances in series, for example from junction to case and from case to surroundings (“ambient”)</li></ul></li></ul> <p>Electronics KTN – Knowledge For Growth</p>	<p>We're starting our search for a compact model by going back to basics. In a semiconductor device the source of heat is the junction, and the heat generated propagates through the internal structure of the device, reaching the surface and leads, and finally being released into the environment by both convection and conduction.</p> <p>The simplest models will have a single thermal resistance from the junction to the surroundings, with all thermal resistances in series, for example first from the junction to the case, and then from the case to the surroundings, usually referred to by the term “ambient”.</p>


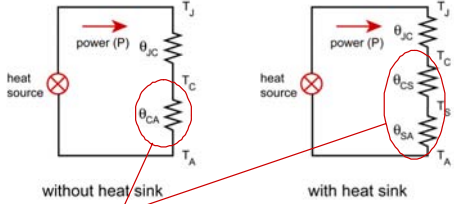

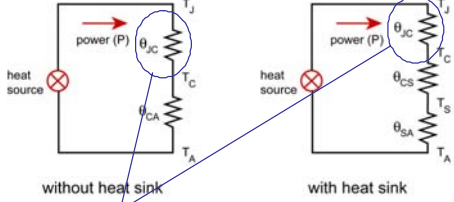

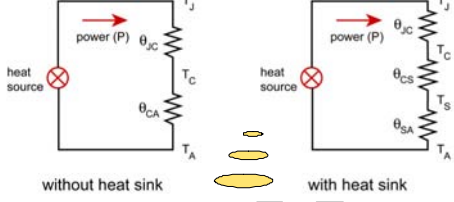

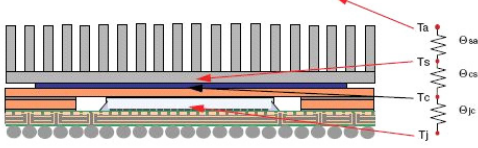
## Modelling heat-generating elements

 <p><b>The one-resistor model</b></p> <ul style="list-style-type: none"> <li>The junction temperature (<math>T_j</math>) can be expressed as</li> </ul> $T_j = T_a + \theta_{JA} \times P$ <p>where</p> <ul style="list-style-type: none"> <li><math>T_a</math> = ambient temperature</li> <li><math>\theta_{JA}</math> = thermal resistance between junction and ambient air</li> <li><math>P</math> = power consumption (i.e. power input)</li> </ul> <p style="text-align: right; font-size: small;">Electronics KTN – Knowledge For Growth</p>	<p>In the one-resistor model, we express the junction temperature rise above ambient as the product of the thermal resistance between junction and ambient air and the power dissipated in the device.</p>
 <p><b>The one-resistor model</b></p> <ul style="list-style-type: none"> <li>The junction temperature (<math>T_j</math>) can be expressed as</li> </ul> $T_j = T_a + \theta_{JA} \times P$ <ul style="list-style-type: none"> <li>The following observations can be made           <ul style="list-style-type: none"> <li>for the same power consumption, reducing the thermal resistance reduces the temperature at the junction, so the device can be used in a higher ambient temperature and conversely</li> <li>if using the device at the same ambient temperature, a reduced thermal resistance allows greater power dissipation</li> </ul> </li> </ul> <p style="text-align: right; font-size: small;">Electronics KTN – Knowledge For Growth</p>	<p>Even this simple equation demonstrates that, for a constant power dissipation, reducing the thermal resistance reduces the temperature at the junction so that the device can be used at a higher ambient temperature. Conversely, using the device at the same ambient temperature, a reduced thermal resistance will allow greater power dissipation.</p>
 <p><b>The one-resistor model</b></p> <ul style="list-style-type: none"> <li>Can only apply when the conditions under which the thermal resistance value was measured are exactly replicated in the application. <b>This is not realistic!</b></li> <li>Need (at least) to analyse the problem into           <ul style="list-style-type: none"> <li>heat paths within the device</li> <li>heat paths from the outside of the device</li> </ul> </li> </ul> <p style="text-align: right; font-size: small;">Electronics KTN – Knowledge For Growth</p>	<p>But of course this will only apply when the conditions under which the thermal resistance was measured are exactly replicated in the application. Bluntly, this is not realistic! So we need to analyse the different thermal paths, and the minimum useable model breaks down the problem into heat paths within the device and heat paths from the outside of the device to the ambient.</p>
 <p><b>The series-resistor model</b></p> <div style="border: 1px solid black; border-radius: 50%; padding: 5px; width: fit-content; margin: 10px auto;"> <p>the values of thermal resistance, and the validity of any models, are critically dependent on the device structure</p> </div> <ul style="list-style-type: none"> <li>Junction: Junction temperature (<math>T_j</math>)           <ul style="list-style-type: none"> <li>Thermal resistance between junction and case (<math>\theta_{JC}</math>)</li> </ul> </li> <li>Case surface: Case temperature (<math>T_c</math>)</li> <li>Ambient air: Ambient temperature (<math>T_a</math>)</li> </ul> <p style="text-align: right; font-size: small;">Electronics KTN – Knowledge For Growth</p>	<p>This series-resistor model makes the simplification that there are only two thermal resistances between junction and the outside world, the thermal resistance between junction and case, and the thermal resistance between case and ambient.</p> <p>The first of these, referred to as <math>\theta_{JC}</math>, is a function of the device, and is pretty much unalterable – once we have chosen a device, we have dictated the parameters of the many thermal paths available between junction and case, although the percentage of heat that goes down any particular path will depend on the application.</p>





## Modelling heat-generating elements

 <h3>The series-resistor model</h3> <ul style="list-style-type: none"> <li>Junction: Junction temperature (<math>T_j</math>)             <ul style="list-style-type: none"> <li>Thermal resistance between junction and case (<math>\theta_{JC}</math>)</li> </ul> </li> <li>Case surface: Case temperature (<math>T_c</math>)             <ul style="list-style-type: none"> <li>Thermal resistance between case and ambient air (<math>\theta_{CA}</math>)</li> </ul> </li> <li>Ambient air: Ambient temperature (<math>T_a</math>)             <ul style="list-style-type: none"> <li>this value depends on the environment and the cooling mechanisms at work</li> </ul> </li> </ul> <p>Electronics KTN – Knowledge For Growth</p>	<p>The second resistor in the series-resistor model is the thermal resistance between case and ambient, referred to as <math>\theta_{CA}</math>, so the total junction to ambient thermal resistance is the sum of the two components. However, in the case of <math>\theta_{CA}</math>, its value depends on the nature of the environment and the cooling mechanisms at work. Unlike the junction to case thermal resistance, case to ambient resistance can be reduced by adding heat sinks, blowing air at the part, or more complex technology.</p>
 <h3>Adding a heat-sink to the device</h3> <ul style="list-style-type: none"> <li>Thermal resistance between junction and case (<math>\theta_{CS}</math>)             <ul style="list-style-type: none"> <li>determined by the structure of the device</li> <li>can be treated as a fixed value</li> </ul> </li> <li>Thermal resistance between case and ambient air (<math>\theta_{CA}</math>) varies greatly according to the mounting conditions</li> </ul> <p>Electronics KTN – Knowledge For Growth</p>	<p>So the <math>\theta_{JA}</math> is two resistances in series, and the simplest model uses that approach. The thermal resistance between junction and case can be treated almost as a fixed value as it is device-dependent, whereas the thermal resistance between case and ambient varies greatly according to the mounting conditions.</p>
 <h3>Adding a heat-sink to the device</h3> <ul style="list-style-type: none"> <li>Thermal resistance between junction and case (<math>\theta_{CS}</math>)             <ul style="list-style-type: none"> <li>determined by the structure of the device</li> <li>can be treated as a fixed value</li> </ul> </li> <li>Thermal resistance between case and ambient air (<math>\theta_{CA}</math>) varies greatly according to the mounting conditions</li> <li>Attaching a heat sink (radiator) adds a heat dissipation route from the case surface through the radiator</li> <li>This is (conceptually) introducing a smaller thermal resistance (<math>\theta_{CS} + \theta_{SA}</math>) via a radiator, in place of the device's original thermal resistance</li> <li>Thus <math>\theta_{CA}</math> is reduced between case and ambient, the amount depending on the characteristics of the radiator</li> </ul> <p>Electronics KTN – Knowledge For Growth</p>	<p>When we modify the heat dissipation route from the case surface, for example by adding a heat sink, we are reducing one of the elements in the total thermal resistance, and thus reducing the thermal resistance between case and ambient. The amount of that reduction depends very much on the characteristics of the radiator.</p> <p>As with the one-resistor model, we then get the option of reducing the temperature achieved, or increasing the dissipation for given conditions. This is the type of consideration that often takes place with “over-clocking” – as the processor clock speed is increased, the power dissipation increases, as this is a function of clock frequency. Reducing the thermal resistance between case and ambient can allow us to run faster.</p>
 <h3>Adding a heat-sink to the device</h3> <div style="display: flex; justify-content: space-around;"> <div style="text-align: center;">  <p>without heat sink</p> </div> <div style="text-align: center;">  <p>with heat sink</p> </div> </div> $\theta_{JA} = \theta_{JC} + \theta_{CA} = (T_j - T_a) / P$ $\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA} = (T_j - T_a) / P$ <p>Electronics KTN – Knowledge For Growth</p>	<p>The effect of adding a heat sink to the device is shown here diagrammatically. Without the heat sink there are two thermal resistances in series, with the heat sink, there are three, representing the fact that heat is travelling from the source at the junction through to the case, and from there through the heat sink to the ambient.</p>


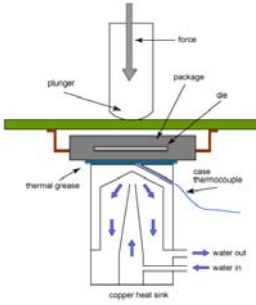



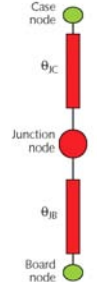
## Modelling heat-generating elements

 <p><b>Adding a heat-sink to the device</b></p>  <ul style="list-style-type: none"> <li>More resistor elements, but total resistance lower, <i>provided</i> <ul style="list-style-type: none"> <li>good connection made between case and sink</li> <li>heat sink is effective</li> </ul> </li> </ul> <p style="text-align: right; font-size: small;">Electronics KTN – Knowledge For Growth</p>	<p>Of course the combination of the two thermal resistances from case to sink and sink to ambient is actually lower than the original <math>\theta_{CA}</math>, because <math>\theta_{CS}</math> can be made low by using a thermal interface material, and <math>\theta_{SA}</math> uses its extended surface to greatly improve the coupling of heat to the ambient. The total resistance will be much lower, provided that good connection is made between the device and the heat sink, and that heat sink is effective.</p>
 <p><b>Adding a heat-sink to a package</b></p>  <ul style="list-style-type: none"> <li>Adding a heat sink may also modify the thermal paths from junction to case <ul style="list-style-type: none"> <li>can't regard this as totally invariant</li> </ul> </li> </ul> <p style="text-align: right; font-size: small;">Electronics KTN – Knowledge For Growth</p>	<p>At the same time that we have added a heat sink to the package and replaced <math>\theta_{CA}</math>, we may find that we have also modified the thermal paths between the junction and the case by encouraging heat flow through parts of the case that are normally not well coupled to the ambient. So we can't regard that thermal resistance as totally invariant. Fortunately, in this case, the value of <math>\theta_{JC}</math> is likely to reduce because of improved contact to cooling surfaces. This unexpected help will be predicted by the detailed model, but not of course by this simple view.</p>
 <p><b>Adding a heat-sink to a package</b></p>  <p style="text-align: center; font-size: small;">as a general strategy, try and identify thermal resistances that can be changed to advantage</p> <p style="text-align: right; font-size: small;">Electronics KTN – Knowledge For Growth</p>	<p>This is only a very simple example, but the way in which thermal resistances can be modified leads us to the useful general strategy that it's worth identifying thermal resistances that we can get access to and which we can change to give our design an advantage. And the example can be extended way beyond the device to the board assembly, the complete equipment and so on. Looking for sources of thermal resistance that can be modified might just trigger a useful idea.</p>
 <p><b>Thermal resistance applied to a PBGA</b></p> <ul style="list-style-type: none"> <li>In this case, the thermal path to ambient becomes more complex</li> </ul>  <p style="text-align: right; font-size: small;">Electronics KTN – Knowledge For Growth</p>	<p>If we apply the thermal resistance idea to a plastic ball grid array, this time with a heat sink mounted to the top surface, we can again draw our electrical analogy, showing the route of the heat from junction to case, through the heat sink, to the ambient. In this case the heat path may be quite lengthy, especially with a face-up chip, although a filler might be used to enhance direct conduction. So we can use this approach to examine the effect of options such as adding a heat sink, although it will be fairly clear that this model is defective, in that it fails to take account of any heat that might be conducted through the balls to the board. It is this thought that will lead to our "two-resistor model" in a few slides' time.</p>

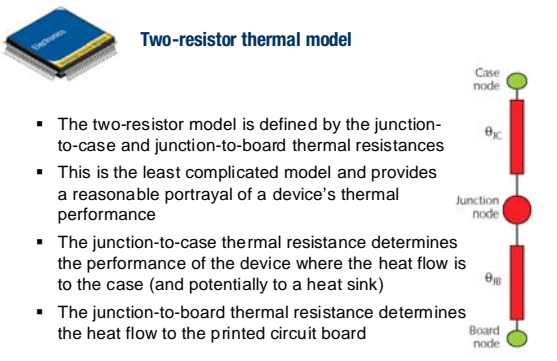
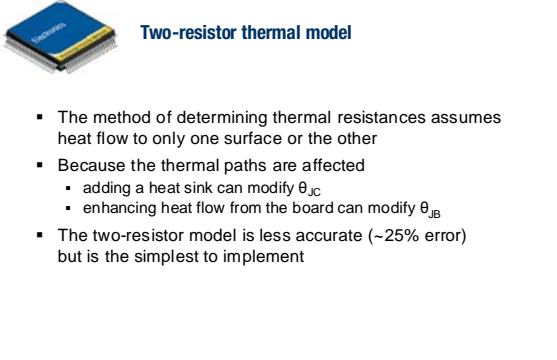
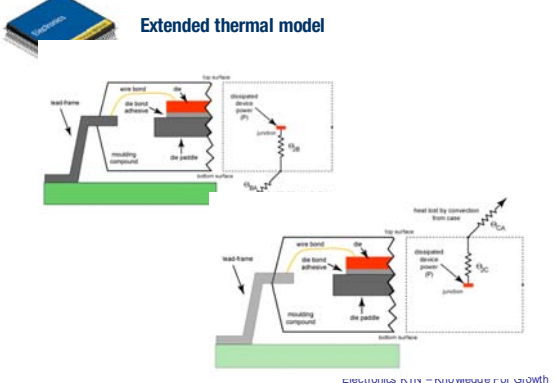
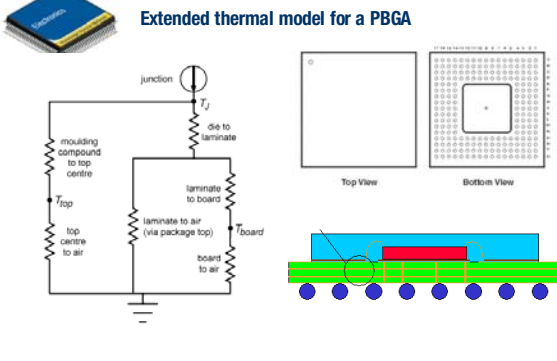
## Modelling heat-generating elements

 <p><b>Quoted values of thermal resistance</b></p> <ul style="list-style-type: none"> <li>▪ <math>\theta_{JA}</math> – junction-to-ambient thermal resistance <ul style="list-style-type: none"> <li>▪ specified on the datasheet</li> </ul> </li> <li>▪ <math>\theta_{JC}</math> – junction-to-case thermal resistance <ul style="list-style-type: none"> <li>▪ specified on the datasheet</li> </ul> </li> </ul> <p><i>we have seen that this is rarely a useful value</i></p> <p><i>just because the data sheet has a value, doesn't mean that it's correct!</i></p> <p>Electronics KTN – Knowledge For Growth</p>	<p>A data sheet might quote different values. You might get a value for junction to ambient thermal resistance, though this should be regarded with suspicion – with so many potential variables, this is rarely a useful value.</p> <p>Also common on data sheets will be a junction to case thermal resistance, although we have seen that its true value will depend on how cooling is being applied to the package – just because the data sheet has a value, it doesn't mean that it is correct!</p>
 <p><b>Quoted values of thermal resistance</b></p> <ul style="list-style-type: none"> <li>▪ <math>\theta_{JA}</math> – junction-to-ambient thermal resistance <ul style="list-style-type: none"> <li>▪ specified on the datasheet</li> </ul> </li> <li>▪ <math>\theta_{JC}</math> – junction-to-case thermal resistance <ul style="list-style-type: none"> <li>▪ specified on the datasheet</li> </ul> </li> <li>▪ <math>\theta_{CS}</math> – case-to-heat-sink thermal resistance <ul style="list-style-type: none"> <li>▪ specified thermal interface material</li> </ul> </li> <li>▪ <math>\theta_{SA}</math> – heat-sink-to-ambient thermal resistance <ul style="list-style-type: none"> <li>▪ specified by the heat sink manufacturer</li> </ul> </li> </ul> <p><i>measurable, but variation in application</i></p> <p><i>dependent on airflow</i></p> <p>Electronics KTN – Knowledge For Growth</p>	<p>The thermal resistance from case to heat sink will be specified by the supplier of the thermal interface material. Its intrinsic value is measurable, but the value of the resulting thermal resistance will depend on factors such as the bond thickness or pressure applied, depending on the type of material.</p> <p>Finally we have the thermal resistance from heat sink to ambient, which will be specified by the heat sink manufacturer, but be dependent on airflow.</p>
 <p><b>Measuring thermal parameters</b></p> <ul style="list-style-type: none"> <li>▪ It is important that <ul style="list-style-type: none"> <li>▪ the package junction temperatures are known as accurately as possible through direct measurement</li> <li>▪ such measurements are repeatable and comparable to measurements made on other packages</li> <li>▪ the measurement technique is an industry standard <ul style="list-style-type: none"> <li>▪ to achieve meaningful and unbiased comparison</li> </ul> </li> </ul> </li> </ul> <p>Electronics KTN – Knowledge For Growth</p>	<p>Whichever package parameters we choose to use, we need to know them as accurately as we can because they make a major impact on the model, and the parameters need to be measured if possible, or at the very least predicted and verified.</p> <p>The requirement is for a standardised technique throughout the industry, so that a designer looking at data sheets gets comparable figures that were measured under the same conditions. Those conditions might not mirror the application exactly, but they do allow a meaningful and unbiased comparison between different devices.</p>
 <p><b>Measuring thermal parameters</b></p> <ul style="list-style-type: none"> <li>▪ It is important that <ul style="list-style-type: none"> <li>▪ the package junction temperatures are known as accurately as possible through direct measurement</li> <li>▪ such measurements are repeatable and comparable</li> <li>▪ the measurement technique is an industry standard</li> </ul> </li> <li>▪ Thermal characterisation standards for the semiconductor industry produced by <ul style="list-style-type: none"> <li>▪ SEMI</li> <li>▪ JEDEC (JESD51 and related standards)</li> </ul> </li> <li>▪ Standards cover thermal measurement and test procedures for a variety of component packages</li> </ul> <p>Electronics KTN – Knowledge For Growth</p>	<p>The earliest test standards were produced by the US military and SEMI, the Semiconductor Equipment and Materials Institute, a US trade organisation. More recently, JEDEC, the Solid State Technology Association, which will probably be familiar to you as the body responsible for standardising semiconductor package outlines, has also been active in creating standards for thermal measurement. Given that there are many different package types and a wide variation in operating conditions, it's not surprising that there are a number of standards.</p>





## Modelling heat-generating elements

 <p><b>Example of a test method</b></p> <p><math>\theta_{JC}</math> is measured with a package on a standard board, but with heat forced to flow through the package surface by putting the package in contact with a water-cooled cold plate, and otherwise insulated from surrounding air.</p> <p>A known amount of power is applied, and the chip and package temperatures are measured.</p>  <p>Electronics KTN – Knowledge For Growth</p>	<p>The aim for all these standards is to have a controlled situation, which combines a degree of realism with an attempt to measure the desired parameter without the influence of extraneous factors. In this example, the board used is a standard board with four layers of copper, made to a JEDEC standard. However, because we are trying to measure junction to case without too much influence from junction-to-board conduction, we force heat to flow through the package.</p> <p>Had we been looking at that conduction to the board, then the case would have been thermally isolated. How this is done you may read for yourself in JEDEC Standard JESD51-8, and how the two figures are used together we will see shortly.</p>
 <p><b>More about thermal models</b></p> <ul style="list-style-type: none"> <li>Most illustrations so far are really one-resistor models <ul style="list-style-type: none"> <li>one (complex) thermal impedance to the package exterior</li> <li>a (series) thermal impedance from package to ambient</li> </ul> </li> <li>Some useful insights into the issues, but are of limited accuracy <ul style="list-style-type: none"> <li>difficult to relate measurements to different situations</li> </ul> </li> </ul> <p>Electronics KTN – Knowledge For Growth</p>	<p>Most of the illustrations we've seen so far are really one-resistor models. That is they have a complex thermal impedance from junction to exterior, in series with a thermal impedance from package to ambient which may have one or more components. They offer some useful insights into the issues, but are of limited accuracy. In particular, it's difficult to relate measurements and the resulting device specifications to the different situations experienced in a real design.</p>
 <p><b>More about thermal models</b></p> <ul style="list-style-type: none"> <li>Most illustrations so far are really one-resistor models <ul style="list-style-type: none"> <li>one (complex) thermal impedance to the package exterior</li> <li>a (series) thermal impedance from package to ambient</li> </ul> </li> <li>Some useful insights into the issues, but are of limited accuracy <ul style="list-style-type: none"> <li>difficult to relate measurements to different situations</li> </ul> </li> <li>We enhance accuracy, though at the expense of added complication, but the models are still "simplified", rather than total reality <ul style="list-style-type: none"> <li>2R model</li> <li>extended models</li> <li>DELPHI models</li> </ul> </li> </ul> <p>Electronics KTN – Knowledge For Growth</p>	<p>We can however, enhance reality in a number of different ways, though at the expense of some added complication. However, the models are still "simplified" rather than total reality. In this next section we will be looking at three ways of doing this: the 2R model, to which we have already alluded, some "extended models", and the thermal models produced by the DELPHI project, which are probably the best approach we will get to an accurate simplified model that has many of the characteristics of the detailed model.</p>
 <p><b>Two-resistor thermal model</b></p> <ul style="list-style-type: none"> <li>The two-resistor model is defined by the junction-to-case and junction-to-board thermal resistances</li> <li>This is the least complicated model and provides a reasonable portrayal of a device's thermal performance</li> </ul>  <p>Electronics KTN – Knowledge For Growth</p>	<p>In the two-resistor model, we are looking at just two paths, from junction to case, concentrating on the outward-facing surface of the package, and then the path from junction through the leads to the board. And we've already indicated how we might measure a device in order to get reasonably accurate values of these parameters.</p> <p>The two-resistor model is probably the least complex one that will allow us to understand how a device will perform thermally. It is particularly suited to straightforward applications, where major cooling efforts are not required.</p>

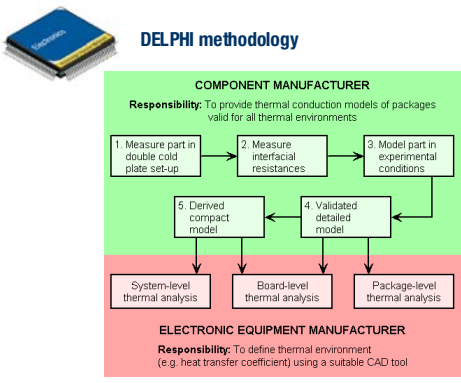

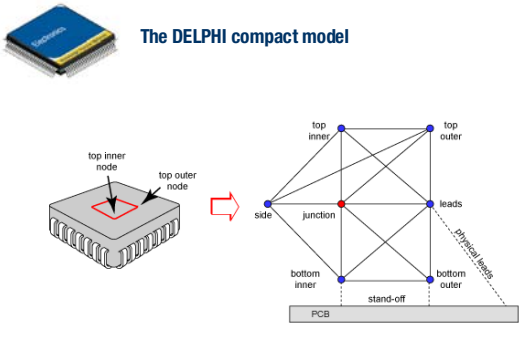
# Modelling heat-generating elements

 <p><b>Two-resistor thermal model</b></p> <ul style="list-style-type: none"> <li>The two-resistor model is defined by the junction-to-case and junction-to-board thermal resistances</li> <li>This is the least complicated model and provides a reasonable portrayal of a device's thermal performance</li> <li>The junction-to-case thermal resistance determines the performance of the device where the heat flow is to the case (and potentially to a heat sink)</li> <li>The junction-to-board thermal resistance determines the heat flow to the printed circuit board</li> </ul> <p>Electronics KTN – Knowledge For Growth</p>	<p>The junction-to-case thermal performance determines how well the device will work when the majority of the heat flow is to the case, and potentially to a heat sink. The junction-to-board thermal resistance determines the heat flow to the printed circuit board on which the device is mounted.</p>
 <p><b>Two-resistor thermal model</b></p> <ul style="list-style-type: none"> <li>The method of determining thermal resistances assumes heat flow to only one surface or the other</li> <li>Because the thermal paths are affected             <ul style="list-style-type: none"> <li>adding a heat sink can modify <math>\theta_{JC}</math></li> <li>enhancing heat flow from the board can modify <math>\theta_{JB}</math></li> </ul> </li> <li>The two-resistor model is less accurate (~25% error) but is the simplest to implement</li> </ul> <p>Electronics KTN – Knowledge For Growth</p>	<p>The problem is that, when it comes to taking measurements, the two heat flows cannot be separated, and the assumption of course is that only one flow is happening at a time, and this is self-evidently not the case. Also, because the values of thermal resistance depend on which thermal paths are preferred, adding a heat sink can modify <math>\theta_{JC}</math>, and enhancing heat flow from the board can modify <math>\theta_{JB}</math>.</p> <p>The two-resistor model is in consequence less accurate than the detailed model, but it is the simplest to implement. So how accurate is it? Well 25% is very much a ballpark figure, but it does reflect the fact that there are a number of uncertainties.</p>
 <p><b>Extended thermal model</b></p> <p>Electronics KTN – Knowledge For Growth</p>	<p>We can extend the idea of a thermal model to include external resistances. In this case, you can see heat removed by conduction through the board and by convection from the top of the case, both modelled in terms of the electrical analogy of thermal resistance.</p>
 <p><b>Extended thermal model for a PBGA</b></p> <p>Electronics KTN – Knowledge For Growth</p>	<p>So far we have just considered the gull-wing package, and heat flow in a BGA is significantly different. But the same approach can be used here to analyse the paths through which heat flows from the junction. Again there is simplification, but we have added complexity, and related each of the parallel paths to physical reality.</p>



## Modelling heat-generating elements

 <h3>Types of models so far</h3> <ul style="list-style-type: none"><li>▪ All are “compact” – thermal network not real component</li><li>▪ Two-resistor – arguably the simplest one that works</li><li>▪ Extended – better mimic of the physical package</li><li>▪ The approach<ul style="list-style-type: none"><li>▪ produces models from which reasonable temperature predictions can be made</li><li>▪ simplifies the system modelling task (compared with the detailed model)</li></ul></li><li>but<ul style="list-style-type: none"><li>▪ has limited accuracy</li><li>▪ the results can vary significantly in different applications (they are boundary dependent)</li></ul></li></ul> <p><small>Electronics KTN – Knowledge For Growth</small></p>	<p>In our search for a compact model, a model that is a thermal network rather than a real component, we’ve looked at the functionality of different networks of thermal resistors. A two-resistor is arguably the simplest one that works, but an extended model may be a better mimic than a physical package. The approach allows reasonable temperature predictions, and simplifies the system modelling task compared with a detailed model. However, the models so far have limited accuracy and the results can vary significantly in different applications. In other words the results are boundary-dependent.</p>
 <h3>Boundary Condition Independence</h3> <ul style="list-style-type: none"><li>▪ A properly constructed detailed model is described as being Boundary Condition Independent (BCI)<ul style="list-style-type: none"><li>▪ model parameters stay constant for all boundary conditions at the thermal contact areas</li></ul></li><li>▪ A BCI model will predict the temperature of the various elements within the package (including junction, case and leads) accurately and regardless of the environment</li><li>▪ Such models are highly desirable!</li></ul> <p><small>Electronics KTN – Knowledge For Growth</small></p>	<p>We have already mentioned the fact that a detailed model is boundary-condition independent, and will accurately predict the temperatures throughout the package regardless of the local cooling environment. In other words, the integrity of the model is such that it can give an accurate result independent of what is happening around it on the printed circuit board. Correct results will be obtained regardless of any local cooling, of whether heat sinks are fitted or fans are blowing direct on the device, or of whether components elsewhere on the board are dissipating power. Such a BCI model is highly desirable, and anything that will give such results without requiring detailed modelling is the Holy Grail of the thermal engineer.</p>
 <h3>The DELPHI project</h3> <ul style="list-style-type: none"><li>▪ Rationale for the development:<ul style="list-style-type: none"><li>▪ the accurate prediction of the operating temperatures of critical electronic parts (at all levels) was seriously hampered by the lack of reliable, standardised input data</li></ul></li><li>▪ DELPHI (<b>D</b>evelopment of <b>L</b>ibraries of <b>P</b>hysical models for an <b>I</b>ntegrated design environment) attempted to address this by the initiation of an industry-wide standard on thermal modelling</li><li>▪ DELPHI is a non-proprietary, open methodology that ran from 1993-96 under funding from the EU</li></ul> <p><small>Electronics KTN – Knowledge For Growth</small></p>	<p>A key step in the search was the DELPHI project. This was an effort to address variations in modelling across the industry, and to encourage standards that would allow the operating temperatures of critical electronic parts to be predicted with sufficient accuracy. The project and its successors attempted to address the problem by initiating an industry-wide standard, and its work was funded by the EU to encourage semiconductor manufacturers to build their own models and put them on line as a resource that would be available for designers to access freely.</p>
 <h3>DELPHI outcome</h3> <ul style="list-style-type: none"><li>▪ DELPHI involves the construction of both detailed and compact models</li><li>▪ DELPHI was followed by a second European project called SEED (<b>S</b>upply <b>E</b>valuation <b>E</b>xploitation of <b>D</b>ELPHI)</li><li>▪ The work carried out in the DELPHI and SEED projects was continued in PROFIT</li><li>▪ A key outcome was a methodology that could be used by component manufacturers to produce validated thermal models to pass on to their customers</li></ul> <p><small>Electronics KTN – Knowledge For Growth</small></p>	<p>What DELPHI did was to build both detailed and compact models, and validate these, and the work involved a considerable amount of effort and two additional tranches of funding. As you will see, the approach is simplified, and the final compact model, while more complex than the two-resistor model, is sufficiently simple that it can be put together fairly rapidly and not be computationally demanding. The way of doing things was a key outcome, and one that could be used by component manufacturers to produce validated thermal models to pass on to their customers.</p>

## Modelling heat-generating elements

 <p><b>DELPHI methodology</b></p> <p><b>COMPONENT MANUFACTURER</b>  <b>Responsibility:</b> To provide thermal conduction models of packages valid for all thermal environments</p> <ol style="list-style-type: none"> <li>1. Measure part in double cold plate set-up</li> <li>2. Measure interfacial resistances</li> <li>3. Model part in experimental conditions</li> <li>4. Validated detailed model</li> <li>5. Derived compact model</li> </ol> <p><b>ELECTRONIC EQUIPMENT MANUFACTURER</b>  <b>Responsibility:</b> To define thermal environment (e.g. heat transfer coefficient) using a suitable CAD tool</p> <p>System-level thermal analysis, Board-level thermal analysis, Package-level thermal analysis</p> <p>Electronics KTN – Knowledge For Growth</p>	<p>This diagram shows the division of responsibilities within DELPHI, where the component manufacturer provides validated models, both detailed and derived, for transmission to the equipment designer in a way that can be integrated within the manufacturer’s design tools at package level, at board level, or at system level, as appropriate. This is a win-win situation, where the equipment manufacturer gets better information in the form that can be easily integrated, and the component manufacturer can give satisfactory information about how the part behaves thermally without having to reveal the detail of the internal construction.</p>
 <p><b>The DELPHI compact model</b></p> <ul style="list-style-type: none"> <li>▪ The DELPHI compact model represents the package as a network of thermal resistors that accurately predicts the junction temperature</li> <li>▪ This network links the junction node to all major surfaces from which heat is extracted</li> <li>▪ Thermal links are also allowed between the surface nodes (shunt resistors)</li> </ul> <p>Electronics KTN – Knowledge For Growth</p>	<p>DELPHI methodology produces both validated detailed models and derived compact models. The latter represents the package as a network of thermal resistors that can be used to predict the junction temperature with a considerable degree of accuracy. The network links the junction node to all the major surfaces from which heat is extracted, and thermal links are also provided across the surface, to model the way in which heat flows – these are the so-called shunt resistors.</p>
 <p><b>The DELPHI compact model</b></p> <p>The diagram shows a PLCC package on the left with nodes labeled 'top inner node' and 'top outer node'. On the right, a network diagram shows a central red 'junction' node connected to blue nodes: 'top inner', 'top outer', 'side', 'bottom inner', and 'bottom outer'. 'Leads' are also connected to the junction. 'Stand-off' nodes are connected to the bottom inner and bottom outer nodes. 'Thermal links' are shown between adjacent surface nodes.</p> <p>Electronics KTN – Knowledge For Growth</p>	<p>The model is indicated in this diagram, which shows a PLCC package. The internal junction is shown as the red node, and other physical parts of the package are indicated by blue nodes. Note that a distinction is drawn between the inner sections of top and bottom surface, corresponding to the area most directly influenced by the die, and the outer regions, which are regarded as a separate node. The junction is connected to each of the nodes by a line representing the thermal resistance – in this case, for simplicity, an electrical resistance has not been shown on the diagram. In addition to the links from the junction node, surface nodes that are physically adjacent are joined by shunt connections, so that the matrix is almost fully interconnected.</p>

## Modelling heat-generating elements

 <h3>The results of DELPHI models</h3> <p>more about this is the associated case study</p> <ul style="list-style-type: none"><li>Two-resistor model predicted the junction temperature rise and heat flux to the board to within approximately 30%<ul style="list-style-type: none"><li>useful for some limited design objectives</li></ul></li><li>Errors of such a magnitude are not acceptable when accurate temperature predictions are required under challenging design constraints</li><li>DELPHI model yielded better than 10% error for both the junction temperature and the heat flux simulations</li><li>Time savings realised by using the DELPHI model over the detailed model were a factor of five or more</li></ul> <p>Electronics KTN – Knowledge For Growth</p>	<p>The DELPHI compact model is far more elaborate than the two-resistor model, but its origins are the same, and it is an extension of the concept which has found favour because it is a relatively simple way of representing complex reality. It's also popular because it appears to give good results. Whilst a two-resistor model can predict thermal performance to an accuracy that is useful for some design work, 30% errors are not acceptable when working near the limits of components.</p> <p>By contrast, the DELPHI model gives accuracies better than 10% in terms of both junction temperature and heat flux simulation. And its time savings are impressive, by comparison, with the DELPHI model converging in less than 20% of the time taken by the detailed model. There is more about accuracy and so on in the associated case study.</p>
 <h3>Making DELPHI work</h3> <ul style="list-style-type: none"><li>Use for modelling the majority of components<ul style="list-style-type: none"><li>make detailed models of challenging or sensitive elements</li></ul></li><li>Access BCI-independent models<ul style="list-style-type: none"><li>information from vendors</li><li>on-line resources</li></ul></li><li>Useful as a basis for constructing your own models</li></ul> <p>Electronics KTN – Knowledge For Growth</p>	<p>High-precision thermal simulation is becoming increasingly important, and the precision of the models, and data embedded in them, has a huge bearing on the accuracy of the simulations. So the DELPHI approach is very effective for modelling the majority of components, although it may still be necessary to make detailed models of challenging or sensitive elements. Fortunately, more information is becoming available both direct from vendors and in terms of on-line resources that have been developed to translate detailed thermal models into compact models. And the concept of the DELPHI model is also of use as a basis for constructing your own models if you are using specialised components, because not everything is available off-the-shelf.</p>